shared memory device is partitioned for storing the address and control information in a first memory array and for storing the data in a second separate memory array.

REMARKS

Before addressing the merits of their response to the last office action, the applicants would like to make the Examiner aware of a related co-pending application, which is identified in the added cross-reference to related application section of the specification. The related application, currently under examination by Examiner R. Phan of Group Art Unit 2305, was subject to a restriction requirement primarily because a first set of claims (Group I claims) were drawn to a dual bus system, classified in Class 395, subclass 308, and a second set of claims (Group II claims) were drawn a buffer for a multiprocessor system running real time processes, classified in class 395, subclass 250. In the co-pending application, the applicants elected the Group I claims for prosecution and cancelled the Group II claims as non-elected claims. Because of the subject matter similarity between the claims of the instant application and the Group II claims, the applicants have decided to prosecute their non-elected Group II claims under the instant application. Accordingly, the applicants have introduced new claims 27-34, which correspond to the Group II claims of the co-pending application. The applicants have also introduced new claims 35-41, which cover some of the more detailed features of their amended claims. The applicants kindly invite the Examiner to examine these new claims along with the pending claims. The applicants thank the Examiner in advance for cooperation in this matter.

The Examiner has objected to the title of the invention for not being descriptive. As reflected above, the applicants have changed the title of their invention to "NON-BLOCKING LOAD BUFFER HAVING MULTIPLE QUEUES FOR TRANSFERRING DATA BETWEEN A NUMBER OF PROCESSORS AND PERIPHERAL DEVICES", a title that is believed to be indicative of the invention to which the claims are directed.

The Examiner has rejected claims 1-26 under 35 U.S.C. as being unpatentable over U.S. Patent 5,043,981 issued to Firoozmand et al. (the Firoozmand patent) in view of U.S. Patent 5,541,912 issued to Choudhury et al. (the Choudhury patent).

The Firoozmand patent discloses an FDD system that transfers multiple priority queues into multiple logical FIFOs of an output buffer through a single physical FIFO. By determining the amount of space available at a particular logical FIFO before a data transfer, the FDD system allegedly prevents "lock up" conditions resulting from residual data remaining in the physical FIFO following each data transfer. The FDD system transfers data from a higher priority queue into a corresponding logical FIFO only if the space available in the logical FIFO is at least equal to the storage capacity of the physical FIFO. Otherwise, subject to space availability, the FDD system allows data transfers from a lower priority queue into its corresponding logical FIFO. Once space becomes available in the previously unavailable logical FIFO, the FDD system resumes the data transfers from the higher priority queue. In FIG. 6, the Firoozmand patent shows a receive FIFO (labeled 175) comprising a queue of data received from a medium, and four transmit FIFOs (labeled 177) comprising a queue of data to be supplied to the medium.

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The Choudhury patent discloses a dynamic threshold system that dynamically varies the length of a plurality of queues based on the space availability of a shared memory space. Choudhury's system reserves a small amount of memory space by not allocating it to the queues. The system allegedly adapts to uncertain or changing load conditions by sharing the reserved space and preventing any single queue from monopolizing the shared memory space at the expense of other queues.

According to the specification, the present invention is incorporated in a data processing system that has one or more requesting processors, which generate processor requests directed to one or more peripheral devices. As amended, the pending claims are directed to a non-blocking load buffer used in such data processing system. The non-blocking load buffer of the invention includes a plurality of variable depth pending queues corresponding to each one of the plurality of peripheral devices, for queuing entries of the processor requests. A variable length return queuing unit queues the data returned from the peripheral devices in response to an outstanding processor request. The load buffer also includes a free pool of entries for placing entries of the outstanding processor request, after the outstanding processor request is accepted by a corresponding requesting processor. The Examiner's attention is respectfully directed to Figure 5 of the drawings and its related disclosure on page 10, lines 25-29 and page 11, lines 1-14, where the applicants have clearly described and shown the internal architecture of the non-blocking buffer of the invention including the variable length pending queue, the return queue, and the free pool of entries.

The applicants respectfully submit that for the reasons stated below the newly amended claims of the instant application are clearly distinguished over the combination of the Firoozmand and Choudhury patents. This is primarily because the combination does not teach a non-blocking load buffer that queues processor requests directed to a plurality of peripheral devices into corresponding variable length pending queues, where the entries of an outstanding processor request are placed into a return queue and where the entry of the return queues is freed up after the outstanding processor request is accepted by a corresponding requesting processor. The Firoozmand patent does not teach or suggest creating a free pool of entries, whatsoever. Consequently, there is no teaching for placing an entry of its receive FIFO 175 in such a free pool. With regard to the receive FIFO, the Firoozmand patent merely states that the FIFO receives data from a medium. FIG. 6 of the Firoozmand patent shows the output data flow of the receive FIFO 175 to be directed into a plurality of link list queues 178. The Examiner's attention is respectfully directed to Firoozmand patent's column 7, lines 16-25, where it states that the link list queues "correspond to the synchronous and three levels of asynchronous priorities." Accordingly, the applicants respectfully submit that the Firoozmand patent does not teach placing the entries of the receive FIFO in a free pool of entries. Moreover, it is the applicants' position that there is no suggestion in the Firoozmand patent for placing the entries of the receive FIFO into a free pool of entries, because the problem being solved by the Firoozmand patent would not have benefited from such placement. The Firoozmand patent allegedly solves the lock up conditions associated

with transferring data through a physical FIFO. The applicants see no benefit in solving lock up conditions by placing the entries of the receive FIFO in a free pool of entries.

The Choudhury patent teaches using a reserved space in the memory to prevent any single queue from monopolizing the shared memory space at the expense of other queues. Although the reserved space may be characterized as a free pool of entries, the Choudhury patent fails to teach adding entries to the reserved space, when an outstanding processor request in a return queue is accepted by a requesting processor. There is no teaching, whatsoever, in the Choudhury patent for a return queue in which data for an outstanding processor request are placed. Furthermore, it is the applicants' position that the Choudhury patent would not have benefitted from such a return queue, for solving the problem of preventing monopolization of the memory in an ATM switch. Therefore, the applicants respectfully submit that the Firoozmand and Choudhury patents can not be properly combined for rejecting the amended pending claims 1-14 and 16-17, and 21-24.

In paragraph 13 of the office action, the Examiner has stated that "[C]laims 18-20, 25 and 26 are the corresponding method claims of claims 1-17 and 21-24, and therefore are rejected under the same rationale." The applicants respectfully disagree. The Examiner's attention is directed to the last element of claim 18, which recites the step of "storing said prioritized memory or I/O transactions in one of said queues having a priority level which is one priority level less than the unique priority level corresponding to said prioritized memory or I/O transactions channeled at said step (b) when the space available in the queues corresponding to said prioritized memory or I/O transactions is exceeded." The applicants respectfully submit that claims 1-17 and 21-24

do not include a corresponding limitation that provides for storing a higher priority transactions in a queue having a lower priority level. Also, having carefully reviewed the Firoozmand and Choudhury patents, the applicants have been unable to find a corresponding teaching or suggestion for this limitation. In fact, for preventing lock up conditions, the Firoozmand patent expressly teaches away from storing higher priority and lower priority transactions in the physical FIFO.

With respect to new claims 27-34, which as explained above are the non-elected claims of the co-pending application, a non-blocking load buffer for a multi-processor system running real-time processes is claimed that includes a memory array for storing data, and a control block for simultaneously performing a plurality of memory or I/O transactions. The applicants respectfully submit that none of the cited references, i.e., the Firoozmand and Choudhury patents, teach a system having a controller for simultaneous performance of memory or I/O transactions in a multiprocessor system that runs real time processes. In addition, none of the cited references teach or suggest using a buffer for queuing processor requests that are non-blocking, and, hence, can be executed simultaneously. Moreover, the problems to which the cited references are directed would not have benefitted from simultaneous performance of the requests. The Firoozmand patent would not have benefited from the simultaneous performance of the requests, when solving the lock up conditions associated with the transfer of data through its physical FIFO. Similarly, in the Choudhury patent, the simultaneous processing of requests would not have benefitted the solution for monopolizing the shared memory space. Therefore,

the applicants respectfully submit that the Firoozmand and Choudhury patents alone or in combination do not anticipate or render claims 27-34 obvious.

The newly added dependent claims 35-41 are directed to some of the more detailed features of corresponding independent claims. Because the applicants believe that all of the independent claims are distinguished over the cited references, they believe that all of the dependent claims are allowable. In view of the above amendments and arguments, the applicants believe that all their pending claims are in condition for allowance, therefore, an early notice of allowance is respectfully solicited.

Respectfully submitted,

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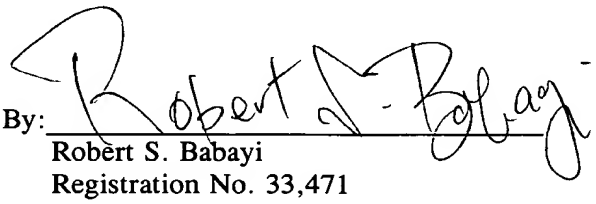
By: 

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